Address: No.4, Baharan St., Golestan1 St., Derakhti Blv., Dadman Ave., Tehran, Iran
Phone: +98 9122401796
Homepage: http://nanolab.ut.ac.ir/FM/Mozaffari.htm
Email: mozaffari.nima@gmail.com

Seyed Nima Mozaffari

Objective:

Pursuing PhD Degree in Electrical Engineering

Education:

Fall 2007 – 2010 **University of Tehran** **Tehran, Iran**

M.Sc., *Circuits and systems, Electronics, Electrical and Computer Engineering.*
Thesis: *Design of Digital Circuits Resistant to Process Variation in Nanotechnology.*
Advisor: *Prof. Ali Afzali-Kusha*
GPA: 17.51/20

Fall 2002 – 2007 **University of Mazandaran** **Mazandaran, Iran**

B.Sc., *Electronics, Electrical Engineering.*
Thesis: *Rotating Antena With Automatic Regulator.*
Advisor: *Prof. Hossein Miar Naimi*
GPA: 15/20

Fall 2001 – 2002 **shahid soltani Pre-University institute** **Karaj, Iran**

Pre-University Certificate in Mathematics and Physics.

Fall 1998 – 2001 **shahid soltani High School** **Karaj, Iran**

High School Diploma in Mathematics and physics, shahid soltani High School (Administrated by National Organization for Development of Exceptional Students, NODET).

Research Interests:

- Low-Power, High-Performance, Digital Circuits and Systems Design.
- Design and Optimization Techniques to reduce Variation in Nano-scale era.
- Implementation of DSP and Communication Systems.
- Yield modeling and optimization in scaled CMOS technologies.
- Modeling and optimization of the circuits considering process variation.
- Process variation aware design.
- Analog/RF IC Design
- Digital RF processor.
- Communication Systems (e.g. OFDM and CDMA Transceiver).
- Design and Implementation of Switching Power supply.
- Mixed Signal Integrated Circuits and Systems.

- Computer-Aided Design of VLSI Circuits and Systems.
- Image Processing, Biomedical Image Segmentation.

Current Research:

M.Sc. Thesis: *Design of Digital Circuits Resistant to Process Variation in Nanotechnology.*

Advisor: *Prof. Ali Afzali-Kusha*

1) Estimating the joint parametric yield with predicting the joint probability distribution function (JPDF) of the gate performance (delay) and power (leakage).
2) Optimizing the above model by extending them to the variations of other parameters. (in progress)

Publications:

1. **Seyed Nima Mozaffari**, and Ali Afzali-Kusha, "Statistical Model for Subthreshold Current Considering Process Variations", *Asia Symposium on Quality Electronic Design (ASQED-2010)*, IEEE 2010, pp. 356–360.
2. Saman Kiamehr, Amir Reza Ahmadi Mehr, **Seyed Nima Mozaffari**, and Ali Afzali- Kusha, "A new Block-based SSTA method considering within-die variation", *2nd Asia Symposium on Quality Electronic Design (ASQED)*, IEEE 2010, pp. 260–263.
3. **Seyed Nima Mozaffari**, Hossein Aghababa, and Ali Afzali-Kusha, "Joint-PDF of Timing and Power of Nano-scaled CMOS Digital Gates due to Channel Length Variation", *IEEE International Conference on Electron Devices and Solid-State Circuits* (EDSSC 2010), IEEE 2010.
4. Hossein Aghababa, **Seyed Nima Mozaffari**, Ali Afzali-Kusha, and Behjat Forouzandeh, "Analytical Modeling of Parametric Yield Considering Variations in Leakage Power and Performance of Nano-Scaled Integrated Circuits", Submitted to ISCAS 2012.
5. Hossein Aghababa, **Seyed Nima Mozaffari**, Ali Afzali-Kusha, and Behjat Forouzandeh, "Accurate Estimation of Joint Probability Density Function of Delay and Leakage for nano-CMOS Circuits", Ready to be submitted to Journal of Zhejiang University-SCIENCE C (Computers & Electronics)

Accomplished Projects and Term Papers:

- Generic carrier-based core model for undoped four-terminal double-gate MOSFETs valid for symmetric, asymmetric, and independent-gate-operation modes, Fall 2009.
- Modeling fixed point FIR filters in MATLAB, Fall 2008.
- Hardware Implementation of 10th Order Low Pass Elliptic Digital Filter, Fall 2008.
- Modeling of a CDMA transceiver in MATLAB/SIMULINK, Fall 2008.
- FinFET I-V modeling and the effects of process variation, Fall 2008.
- multi-walled CNT (MWCNT) Interconnect in Memory Technology, Fall 2008.
- Optimizing of clock skew in clock distribution, Fall 2007.
- Design of a 100 MS/sec Sample & Hold Circuit, having THD better than 74dB in different corners in 0.18μm technology, Fall 2007.
- Design of high precision voltage Band Gap in 0.18μm technology, Fall 2007.
- Simulation of Clock distribution network used in Xilinx Virtex-II FPGA for optimizing

clock skew between logic blocks, Fall 2007.

- Low power cache/cache memories, Fall 2007.

Research Experiences:

Oct. 2007 – Present **University of Tehran**

Research Assistant, *Low-Power, High-Performance, Nano-Systems Laboratory*
Advisor: *Prof. Ali Afzali-Kusha*
http://nanolab.ut.ac.ir

- Low-power and high performance digital circuit and system design in deep sub-micron technologies.
- Statistical timing and power analysis methods.
- Statistical delay, power, yield modeling.
- High speed adder/multiplier design.
- Communication system modeling.
- Effects of PVT process corners on performance of a circuit.
- Verilog Switch-level modeling of digital circuits.
- Verilog RTL modeling of digital systems.
- MATLAB and Simulink system level modeling and computer simulations.
- Verilog modeling of digital filters and FFT engines.
- System-level modeling and HDL coding of complex DSP systems, test bench development and their implementation.
- Comparing different proposed low-power logic styles.
- Advanced MOSFET I-V Modeling.

M.Sc. Courses:

Low-Power Integrated Circuits (16/20)
Analog Integrated Circuits Design (16/20)
Nano Devices and Their Integration (18/20)
Advanced VLSI (16/20)
Special Topics: Quantum Computing (19.25/20)
Custom Implementation of DSP systems (17.1/20)
Theory and Technology of Silicon Devices(16/20)
Semiconductor Devices (18.5/20)
MSc Seminar (19.5/20)
MSc Thesis (18.5/20)

Course Presentations:

- "Investigation of the design of digital circuits, resistant from process variation in nanotechnology", Presentation in *MSc Seminar Course*, University of Tehran, Sept. 2009.
- "Optimizing clock skew in clock distribution network", Presentation in *Advanced VLSI Course*, University of Tehran, Dec. 2006.
- "Combined GPS and CDMA in a mobile transceiver" Presentation in *Custom Implementation of DSP Systems Course*, University of Tehran, June 2008.
- "A zero-crossing-based 8b 200MS/s pipelined ADC" Presentation in *Analog Integrated Circuits Design Course*, University of Tehran, Dec. 2007.

Language Proficiency:

Languages: Native speaker Persian, Fluent in English, familiar with Arabic.
TOEFL: Will be held on Jan, 2012.
GRE: Verbal 320, Quantitative 760, Analytical Writing 2.5

Computer Skills:

Programming Languages:
MATLAB, Simulink, Verilog HDL, Basic, 8085/8086/8051 Assembly Language
CAD Tools and HDL:
HSPICE, PSPICE, ORCAD, LEDIT, SEDIT, ModelSim, Leonardo Spectrum, Quartus, Codevision, Protel DXP, Design Compiler, R 2.8.0, SoC Encounter.
Operating Systems and Microsoft Office:
Windows, Linux, MS-DOS, Word, Power Point, Excel, Front-Page

Work Experiences:

- Working on industrial automation system design, 2007-2008.
- Working on PLC, HMI, AVR, FPGA and data transfer fieldbus foundation.
- Design of a Full-Option Digital Timer by wireless module for industrial consumption, 2011.
- Lecturer of "Electronics I", "Pulse Technique", "Logic Circuits", and "Digital Logic", Undergraduate Courses for Electrical Department of Rouzbahan University of Higher Education, Sep.2010 – present.
- Lecturer of "Eng. Math", Undergraduate Courses for Electrical Department of Salehan University, Sep.2011 – present.

Extracurricular Activities and Interests:

- Playing Football, Mountain Climbing, Biking, Hiking, Driving, Music, Movies, Swimming, cooking.

References:

▪ Prof. Ali Afzali-Kusha	*Professor*	University of Tehran	afzali@ut.ac.ir
▪ Prof. B. Forouzandeh	*Associate Professor*	University of Tehran	bforooz@ut.ac.ir
▪ Prof. R. Ghaderei	*Assistant Professor*	University of Mazandaran	r_ghaderi@ut.ac.ir