Curriculum Vitae
Farzan Jazaeri

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Objectives and Major Interests

Working on modeling of junctionless devices (JL DG MOSFETs, nano-wires and VeSFETs).

Education

December 2011-Up to now — **EPFL** — **Lausanne,Switzerland**
PhD, Modeling of Junctionless multiple gate transistors and VeSFTs.

Fall 2006-Jan 2009 — **University of Tehran** — **Tehran, Iran**
M.Sc., Circuits and Systems, Electronics, Electrical Engineering
Thesis: Design of low-power and high performance integrated circuits based on novel devices in nano technologies.
GPA: 18.1/20

Fall 2001-2006 — **K.N.Toosi University of Technology** — **Tehran, Iran**
B.Sc., Electronics, Electrical Engineering
Thesis: Analysis and design antennas & impedance matching circuits in submillimeter wave detectors using Josephson fluxonic diode.
Advisor: Prof. Farshid Raissi,
Prof. M.S.Abrishamian

Fall 2000-2001 — **Roshd college** — **Tehran, Iran**
Pre-University, Certificate in Mathematics and Physics, **GPA:** 19.9/20 (first rank).

Research Interests

Advanced Semiconductor Modeling

- Low-power and high performance VLSI circuits and systems based on nano-scale semiconductor devices and Power-estimation and optimization techniques in low power circuits and systems.
- 3D Device simulation, solid-state physics and nanoscale CMOS devices modeling.
- Working on silicon nanoscale semiconductor devices (DGMOS, FinFET, nano scale Field Effect Diode) which have superior characteristics compared to regular MOS transistors at device lengths below 80 nm.
- Superconductivity, Soliton transistor, wave detection using Josephson fluxonic diode.

Nano-Spectroscopy based on (STM, AFM, Magnetic AFM, EFM and Piezoresponse Mode AFM)
Growth methods of Nano-Organics (Fullerence and CNT), top-down methods and Nano-Lithography
Quantum structures, SET and RTD, Quantum Optics and Photonic Transistors

Honors

- **Patent**
  - **F.Jazayeri**, "A new method to optimize analog/digital circuits and systems based on novel devices", Patent No. 32/07437, Jun. 2009, Iran.
- Ranked 6th among 24 M.Sc. students of the Electrical/Electronics engineering of the University of Tehran, class of 2007.
- Ranked in 0.02% among more than 12,000 students in nation-wide M.Sc. entrance exam in 2006.
- Ranked in 12th among more than 300,000 students in the B.Sc. entrance exam of Azad University in 2001.
- Ranked in 0.1 % among more than 550,000 students in the B.Sc. entrance exam in 2001.
- Ranked 1st in the final pre-university and high school exams in the city of Tehran in 2001.

Selected Publications

Journal papers

1. A.Koukab, **F. Jazaeri**, J-M. Sallese, "On Performance Scaling and Speed of Junctionless Transistors," *Solid-State Electronics*, in press, August, 2012.

2. **F. Jazaeri**, L.Barbut, A. Koukab, J-M. Sallese, "Analytical Model for Ultra-Thin Body Junctionless Double Gate MOSFETs in Subthreshold Regime," has been submitted to *Solid-State Electronics*, November, 2012.

3. **F. Jazaeri**, L.Barbut, J-M. Sallese, "Analytical Approach to Estimate Intrinsic off Current Range in Junction-less Double Gate MOSFET," has been submitted to *IEEE Transaction Electron Devices*, November, 2012.

4. L.Barbut, **F. Jazaeri**, Didier Bouvert and J-M. Sallese, "Transient Off-Current and Inversion Layer Formation in Junctionless FETs," has been submitted to *IEEE Transaction Electron Devices*, December, 2012.

5. **F.Jazayeri**, B.Forouzandeh, and F.Raissi, "Low-power Variable Gain Amplifier with Wide UGBW based on Nanoscale Field Effect Diode," *IEICE Electronics Express*, Vol.6, No.1 pp.51-57, January 2009.

6. **F.Jazayeri**, F.Raissi, B.Forouzandeh, "Low-power and high-performance Automatic Gain Control systems based on nanoscale Field Effect Diode and SOI-MOSFET, " *IEICE Electronics Express*, Vol.7, No.5 pp.371-376, February 2010.

7. **F.Jazayeri**, A.Sammak, and F.Raissi, B.Forouzandeh, "A novel ultra-low-energy sub-threshold inverter based on nanoscale Field Effect Diode," *IEICE Electron. Express*, Vol. 7, No. 13, pp.906-912, March 2010.

8. **F.Jazayeri**, B.Forouzandeh, F.Raissi, "Low-power Double Edge Triggered Flip-Flop based on nanoscale Field Effect Diode," has been accepted by *IEICE Electronics Express*, February, 2010.

9. **F.Jazayeri**, B.Forouzandeh, F.Raissi, "A novel low-energy sub-threshold NAND based on nanoscale Field Effect Diode," has been accepted by *IEICE Electron. Express*, January 2011.

Conference papers

10. **F.Jazayeri**, B.Forouzandeh, A.Jalili, A.Sammak, F.Raissi, "Nanoscale Field Effect Diode as a High Frequency and Ultra Low-power Variable Gain Amplifier in AGC Circuits," *the 20th IEEE International Conference on Microelectronics (ICM08)*, pp. 317-320, Dec. 2008, UAE.

11. **F.Jazayeri**, S.Soleimani, B.Ebrahimi, F.Raissi, B.Forouzandeh, H.R.Ahmadi, "Pseudo-Linear Automatic Gain Control System based on Nanoscale Field Effect Diode and SOI-MOSFET," *the 3rd IEEE International Design and Test Workshop (IDT08)*, pp. 154-158, Dec. 2008, Tunisia.

12. **F.Jazayeri** and Ali-Afzali-Kusha, "Double Edge Triggered Feedback Flip-Flop based on Independent Gate FinFETs in 32nm Technology," *the 4th IEEE SPIE European International Symposium on Microtechnologies*, May 2009, Germany.

13. **F.Jazayeri** and Ali-Afzali-Kusha, "High-Performance and Low-Power of Double Edge Triggered Flip-Flops with Feedback based on nanoscale FinFET Technologies," *the International MultiConference of Engineers and Computer Scientists* 2009 (IMECS 2009).

14. **F.Jazayeri**, Zargar ershadi, "Advanced Engineering Mathematics and Methods to Solve PDEs with Matlab," *K.N.Toosi ECE Press*, 2005, Iran.

Teaching and Working Experiences

Teaching experiences

- Teaching Assistant, Ordinary Differential Equations Course and Methods to Solve the PDEs with Matlab, K.N.Toosi University of Technology, and spring 2003, Dr.Haghighi.
- Teaching Assistant, Ordinary Differential Equations Course, K.N.Toosi University of Technology, fall 2003, Dr.Aghigh.
- Teaching Assistant Advanced Engineering Mathematics Course, K.N.Toosi University of Technology, fall 2003, Dr.Zargar.
- Teaching Assistant, Advanced Engineering Mathematics Course, K.N.Toosi University of Technology, spring 2004, Dr. Mo'tamedi.
- Teaching Assistant, Logic Circuits Design Course, K.N.Toosi University of Technology, spring 2004, Dr. Hosseini-nezhad.
- Teaching Assistant, Signals and Systems Processing Course, K.N.Toosi University of Technology, Fall 2004, Dr. Abrishamian.

- Teaching Assistant, Electronic Circuits Course, K.N.Toosi University of Technology, spring 2005, Dr. Hosseini-nezhad.
- Teaching, VLSI systems design, spring 2009.

Working Experiences

- Samim Rayaneh Company (Jun 2009-January 2010)
    - Working as a software and hardware team programmer and contributing in the design, development and test of broadcast systems.
- R&D engineer for Tehran Regional Electric Co. (TREC), Ministry of Energy (January 2010 – November 2011)
    - Working as a SCADA expert.

Graduate Courses

- Beyond CMOS devices,IMEC, Leuven, September 2012 (PhD)
- Modeling micro/nano-field effect electron devices, Lausanne, August 2012(PhD)
- Integrated circuits technology, Lausanne, December, 2012 (PhD)
- Modeling of emerging electron devices, Lausanne, December, 2012 (PhD)
- Quantum Electronics and solid state, Tehran, Fall 2010 (PhD)
- Nano-Electronics, Tehran, Fall 2010 (PhD)
- Superconductivity, Tehran, Fall 2010, (PhD)
- Nano-Organics, Tehran, Spring 2011, (PhD)
- Advanced Semiconductor Devices, Prof. Afzali-Kusha, ECE University of Tehran, Fall 2006
- Semiconductor Devices Fabrication, Prof. Fathi-pour, ECE University of Tehran, Fall 2006
- Nano Devices and their integration Prof. Afzali-Kusha, ECE University of Tehran Spring 2007
- Low Power IC Design, Prof. Afzali-Kusha, ECE University of Tehran Spring 2007
- Silicon on Insulator (SOI) devices and circuits, Prof. Foruzandeh, ECE University of Tehran, Fall 2007
- Solid state Physics Prof. Mohajerzadeh, ECE University of Tehran, Fall 2007
- Optoelectronic Prof. Afzali-Kusha, ECE University of Tehran, Fall 2007
- Analog IC Design Prof. Shoaie, ECE U of Tehran, Fall 2006

Accomplished Projects & Term Papers

- Working on poly crystalline high mobility thin film transistors.
- Extraction fit models for novel devices (current-voltage curves).
- Performance estimation of digital circuits using circuit simulators and comparison different proposed low-power logic styles.
- Advanced MOSFET, nano scale SOI and FED devices modeling.
- Using nano scale Field Effect Diode in ultra Low-Power and high performance digital and analog designs (Variable Gain Amplifiers in AGC systems).
- High performance and Low-Power of Double Edge Triggered Flip-Flops based on nano scale FinFET technologies.
- Advanced MOSFET I-V Modeling.
- Standard cell layout design and characterization.
- Modification gate leakage model parameters of Predictive Technology Models (PTMs).
- Submillimeter wave detection using Josephson fluxonic diode.
- Implementing of DCT, DST & Gabor transformation on Programmable Function Arrays.
- Worked on Controller Area Network (CAN).

- MATLAB and Simulink system level modeling and computer simulations.
- Analysis and measurement of signal distortion in RF application.
- Mapping of DSP algorithms on Field Programmable Function Arrays.
- Designing Patch and dipolar Antennas and impedance matching circuits design based on superconductor antennas.

Special Skills

- **CAD Tools**
  TCAD, Mdraw, PSPICE, Dessis, ModelSim, HSPICE, ORCAD, Microwave Office, PiscesIIB, Protel, AutoCAD.
- **Programming Languages**
  MATLAB, Verilog HDL, VHDL, C++, Visual Basic, 80592/80196/8051/AVR Assembly Languages.
- **Operating Systems and Microsoft Office**
  Windows, MS-DOS, Word, Power Point, Excel, Front-Page
- **Theoretical skills**
  Strong mathematics, Theoretical background in Communication Systems, Probability and Statistics

Memberships

- IEEE Student member.
- Member of IEEE Circuits and Systems, Communications, Computer, Electron Devices, Laser and Electro-Optics, Signal Processing and Solid-State Circuits Societies.

Abstract of M.Sc. Thesis

Power optimization techniques in low power latches and Flip Flops are widely used in modern VLSI circuits. Double gate devices and circuitry techniques can be used to reduce power consumption and improve Flip Flops performance. In this thesis, a low-power circuit optimization technique for Double-Gated FinFETs with Independent Gates is developed. We optimized Double-edge triggered Feedback Flip-Flop (DFFF), a Hybrid Latch Flipflop (HLFF), Semi Dynamic Flip-Flop (SDFF) and Low Swing clock Double Edge Flip-Flop (LSDFF) based on Independent Gate FinFET and CMOS technologies. In this way using Double-Gated FinFETs technology leads to reduce the number of transistor, save area and power consumption. So we suggest "Doubled Edge Triggered Feedback Flip-Flop" based on Nano Scale FinFET technology (DFFF-FinFET) as the best choice to improve the power-delay Product (66%) in comparison with CMOS process.

As semiconductor industry pushes toward nanosize gate lengths, the need for alternative structures becomes more imperative as MOS performance undergoes degradations due to short channel effects. Among proposed alternative structures modified field effect diode (FED) seems to be specifically suited for variable gain amplifier circuits. Simulation results are provided for the modified nanoscale Field Effect Diode (FED) used as a variable gain amplifier in automatic gain control systems. Field Effect Diode is similar to regular MOS transistors with the exception of using two gates over the channel region and oppositely doped source and drain. Its current-voltage characteristic results in large gain, low power dissipation and better frequency response compared with automatic gain control systems based on regular CMOS transistors. An added feature is the lack of short channel effects in Field Effect Diodes.

National Languages

- Native speaker Persian, Fluent in English and familiar with Arabic, French
- **TOEFL**: (PBT)560

References

Updated list available on demand.

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